

# AutoAmp : An Open-Source Analog Amplifier Design Tool - For Classroom and Lab Purposes

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**Abstract**

This correspondence presents an open-source tool *AutoAmp* developed at the Indian Institute of Technology, Guwahati. It is available at <http://sourceforge.net/projects/autoamp-iitg/>. This tool helps the user to design different types of electronic amplifiers, using solid state devices, for a given specification. It can handle several types of designs namely common-emitter BJT amplifier (single and two-stage), operational amplifiers (inverting and non-inverting) and power amplifier. Not only does it design the amplifier, it also simulates the designed amplifier using SPICE simulator and displays the performance curves. This tool is deemed to prove invaluable in undergraduate teaching and labs. Especially in electronics-design related laboratories, the student need not design the amplifiers which are mostly the heart of many electronic designs.

## I. INTRODUCTION

Analog amplifiers are the building blocks of many electronic circuits. Different types of analog electronic amplifiers are commonly used in radio and television transmitters and receivers, high fidelity (hi-fi) stereo equipment, micro computers and other electronic equipment. Transistor amplifiers are among the most commonly used kinds of amplifiers. Most common active devices used in transistor based amplifiers are bipolar junction transistors (BJTs) and metal oxide semiconductor field-effect transistors (MOSFETs), with BJTs being a preferred choice for lab level circuit-design. BJT based amplifiers find use in audio amplifiers in a home stereo or public address system, RF high power generation for semiconductor equipment, RF and microwave applications such as radio transmitters. An operational amplifier (*op-amp*) is an amplifier circuit with very high open loop gain and differential inputs which employs external negative feedback for control of its transfer function and gain. These attributes form the basis for op-amp applications in integrated circuits and its extensive study and use in experimental circuits.

We have developed a simple open-source amplifier design tool, named AutoAmp, [1] for the following types of amplifiers, given some design specifications:

- 1) Single Stage BJT CE Amplifier
- 2) Two-Stage BJT CE Amplifier
- 3) Operational Amplifier: Inverting/Non-Inverting
- 4) Op-Amp Difference Amplifier
- 5) Class-A Power Amplifier

For each type of design the software requires minimum design specifications assuming the lab working environment. The assumptions can however be modified in the source code as per requirements. Net voltage gain is the key design parameter that the software uses across most amplifier types. However, few designs require more specific information like the maximum available resistance in the case of operational amplifier design; power transmitted to load,  $V_{CC}$  and load resistance in the case of power amplifier. Given the choice of type followed by minimum design specifications, the software generates a netlist file to be opened in LTSpice™ [2] for necessary circuit analysis. AutoAmp is open-source and can be run on both

Windows and Linux-based systems. The necessary adaptations for the OS are mentioned in the AutoAmp website [1]. Autoamp is available for free (along with the source code) at [1].

There are not many free tools which automatically design basic amplifier circuits given the design specifications. It is expected that industries may be maintaining customized circuit design tools to solve their purpose. However use of such commercial tools for academic purposes is likely to be prohibitively expensive. Basic amplifier-circuit design along with its analysis is required in any complex circuit in electronics. Thus availability of such a tool will be a boon for teachers and students alike.

Among the existing tools for amplifier circuit design, tools for operational amplifiers are available, including online tools, like [3], however, there is no open-source design tool available for designing amplifier circuits with BJT amplifiers and class-A power amplifiers. Most importantly, none of the available tools have a provision for the analysis of the circuit generated. We aim to provide an interface where the user can get the design of the circuit in LTSpice™ after providing certain design specifications. Such a tool will be very useful in classrooms and for other non-industrial purposes where such circuit design is warranted.

The existing design tools are pretty complicated (especially for classroom purposes), difficult to use, expensive, not open-source (user cannot change the source to suit his own purpose) and lack a Spice or similar interface. Moreover, design tools for BJTs, power amplifiers are very hard to find. The commercial tools come with a whole package of electronic design automation tools with lot of circuit-options, which makes them complicated. For learning or teaching a course in analog electronics, only a few numbers of these circuits are required. Further, addition or deletion of components and changing the source according to individual requirements can not be done.

Our design tool tries to overcome most of these problems. It is a simple and user-friendly tool. AutoAmp is easy to operate, takes minimum input and generates an LTSpice™ netlist which can be used to design the circuit in LTSpice™ directly. Being open-source, customized changes can be easily made to the source code to give the desired results; components can be easily added or removed by writing some extra functions in the source code.

Section II describes our design approach in detail including the software design methodology and the circuit design approach. Section III shows our demo/experimentation results and includes screenshots from the working of the tool. The elaborate theoretical and mathematical analysis for each type of amplifier can be found in the Appendix A . Section IV sums up the proposal in the conclusion and talks about possible future work related to the tool.

## II. DESIGN APPROACH

This section describes our design approach of the tool in detail. A blackbox representation of the tool is given by Fig. 1.

### A. Software Design Methodology

The tool is a command line software designed in C++ programming language. The program has a class named autoAmp which consists of various functions for computation of the amplifiers' components and one function for printing in the file. A struct data type is defined to store all the computed values and is finally used to create the output file. The user is asked for the name of the input file, to select an amplifier of her choice in a menu based environment and finally to enter voltage gain and other parameters based on the type of amplifier chosen. Based on user's choice the respective functions are called which compute the values of components and store then into the struct defined. Now another function uses this struct to create the netlist of the respective type of amplifier into the file specified by the user in the beginning.

### B. Circuit Design Approach

1) *Single Stage BJT CE Amplifier*: We have a designed a small-signal voltage amplifier operating in the audio frequency range. We have used an n-p-n transistor, namely, 2N2222. Two port h-parameters are

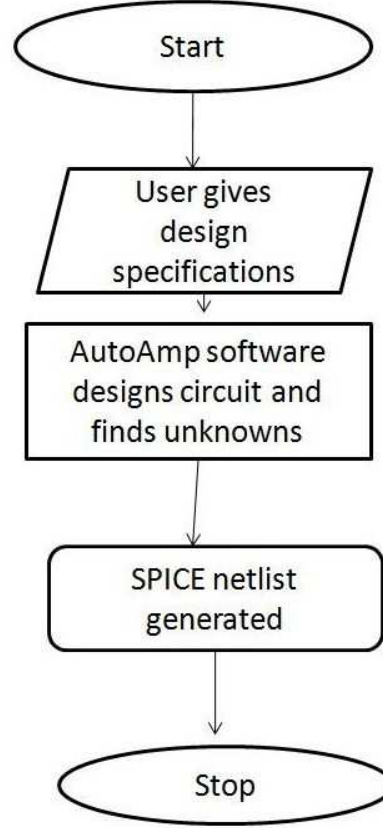


Fig. 1. Blackbox Diagram for AutoAmp

used for circuit analysis. Maximum, minimum, and typical values as required, of the h-parameters are obtained from the transistor datasheet [4]. One method for obtaining the hybrid parameters of the BJT amplifier is given by Al-Zobi et al [5]. These values along with the other known values are used by the software to get optimized values of the circuit components, i.e., resistances and capacitors. The detailed theoretical and mathematical analysis for this part can be found in the appendix A.

2) *Two Stage BJT CE Amplifier*: This design consists of two CE amplifier stages in cascade. Two amplifying stages thus give us a higher overall gain. The design methodology remains the same as in single stage CE amplifier but is applicable over two stages in this case. The detailed theoretical and mathematical analysis for this part can be found in the appendix B.

3) *Operating Amplifiers*: This is the simplest amplifier designing strategy in which we are using the inverting and non-inverting configurations of the ideal Universal OpAmp2 (as given in LTSpice™). The detailed analysis is given by Sedra and Smith [6]. Assuming an ideal op amp with infinite open-loop gain,  $R_{in} = R_1$ . Now to avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. In the case of the inverting op-amp configuration we are studying, to make  $R_{in}$  high we should select a high value for  $R$ . However, if the required gain  $\frac{R_2}{R_1}$  is also high then  $R$  could become impractically large (e.g. greater than a few megaohms). Hence in our design we use a different feedback mechanism by which the circuit is able to realize a large voltage gain without using large resistances in the feedback path. The details of the design can be found in the Appendix. Standard circuit design can be used for the non-inverting input configuration as the input resistance is infinity as desired. The detailed theoretical and mathematical analysis for this part can be found in the appendix C.

4) *Op-amp Difference Amplifier*: In this design, we implement a difference amplifier again using Universal OpAmp2 that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs. The circuit design uses four resistances. The detailed theoretical and mathematical analysis for this part (along with the circuit diagram) can be found in the appendix D.

5) *Class-A Power Amplifier*: Here we have designed a power amplifier by simply implementing a CE BJT amplifier with a high power output stage for which a transformer is used. The detailed theoretical and mathematical analysis for this part can be found in the appendix E.

### III. DEMONSTRATION

Here are some screenshots which are obtained after the netlist file created by AutoAmp is input to LTSpice™. We simulated the netlist files generated by AutoAmp in LTSpice. The input-output voltage graphs for sinusoidal input voltages are presented in the figures 2 - 6. Figure 2 shows a voltage gain of 20 for an input of  $20\text{mV}$  peak-to-peak in single-stage BJT amplifier. Figure 3 shows a total voltage gain of 100 for an input of  $0.5\text{mV}$  peak-to-peak in a two-stage BJT amplifier. Figure 4 and Figure 5 show a voltage gain of 10 for an input of  $20\text{mV}$  peak-to-peak in inverting and non-inverting operational amplifier. Figure 6 shows the graph of voltage gain for difference operational amplifier.

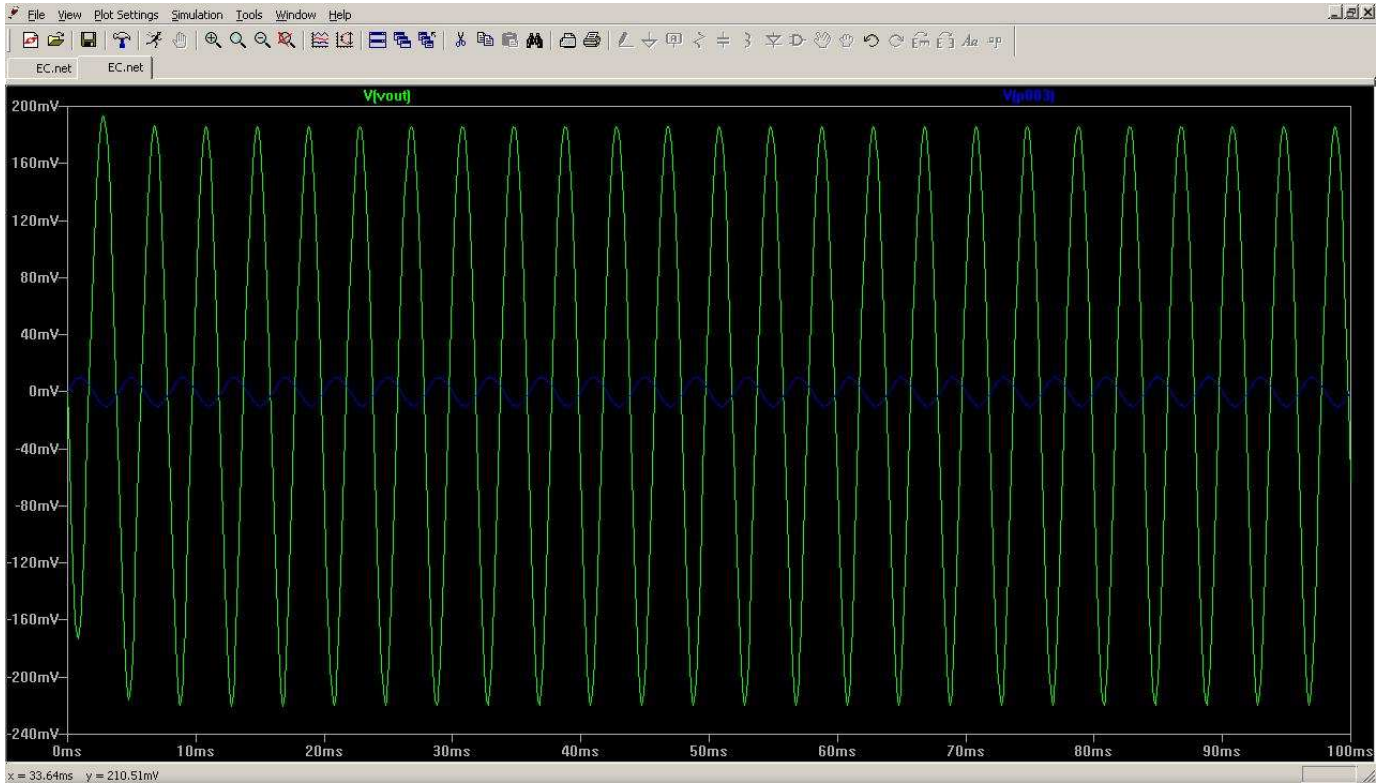


Fig. 2.  $V_{in}$  v/s  $V_{out}$  in BJT Single stage Amplifier

### IV. CONCLUSION

This paper presents a simple open-source design tool using C++ which can help in designing and analyzing an amplifier given some design specifications. The software is able to demonstrate five design spec-combinations. The complete package is deemed to be of utility to circuit designers and instructors, especially in a technical college environment.

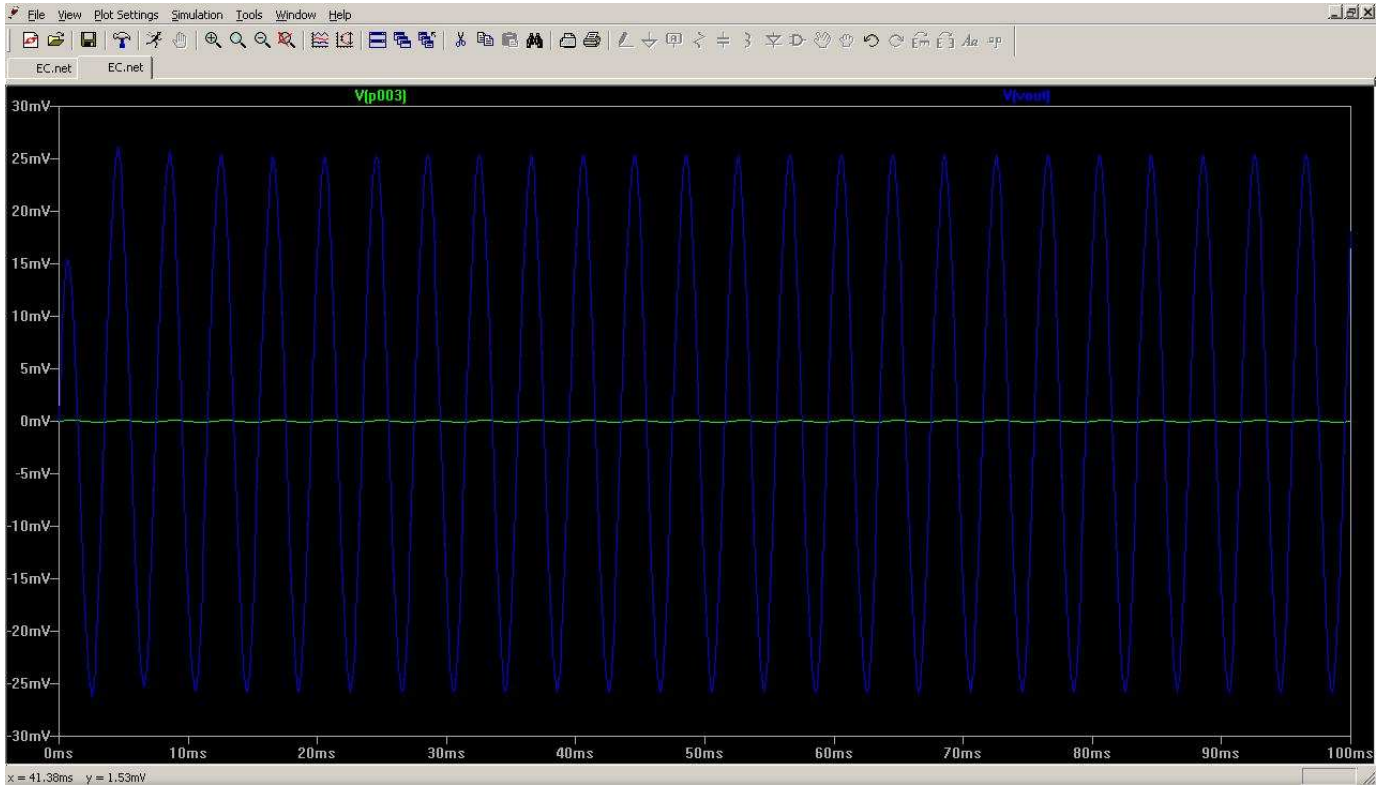


Fig. 3.  $V_{in}$  v/s  $V_{out}$  in BJT two-stage Amplifier

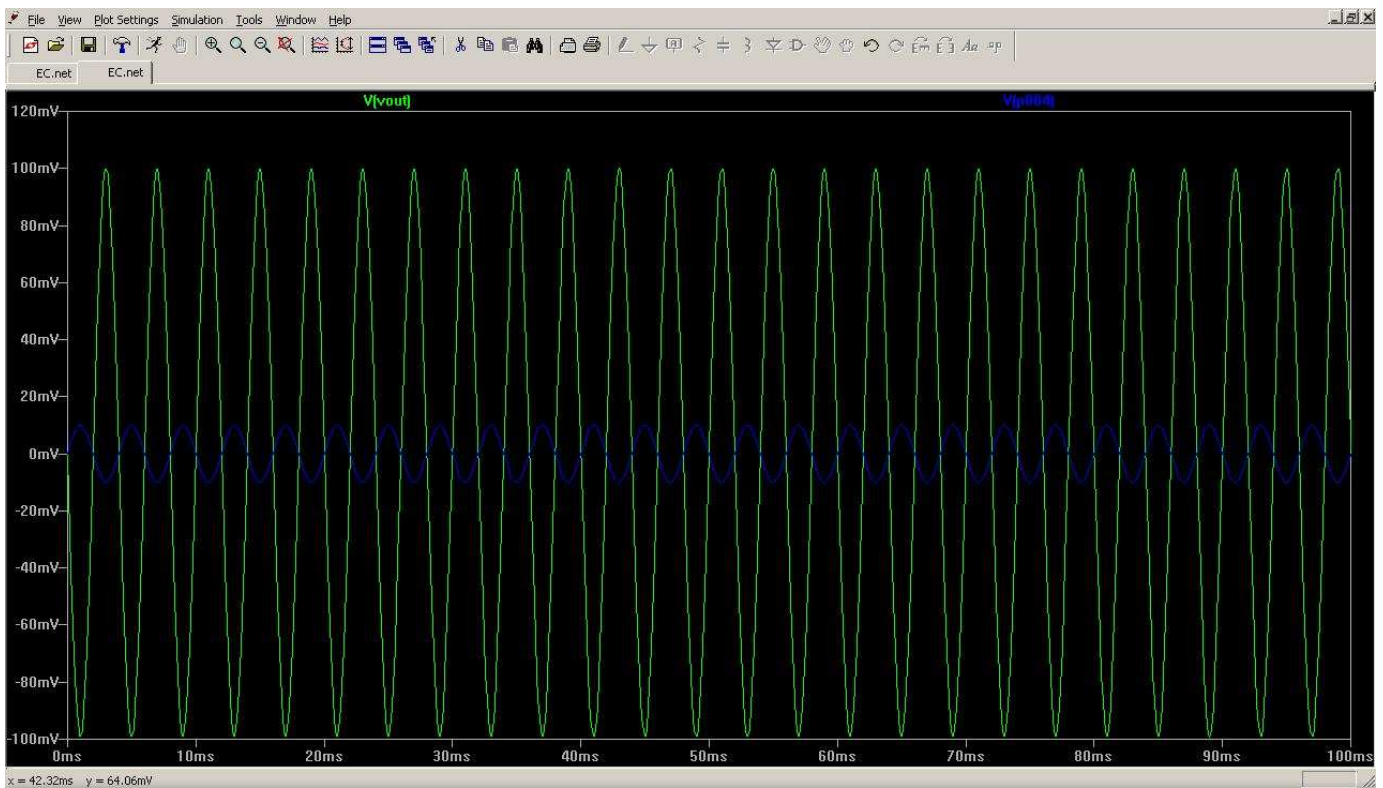


Fig. 4.  $V_{in}$  v/s  $V_{out}$  in Inverting Op-amp

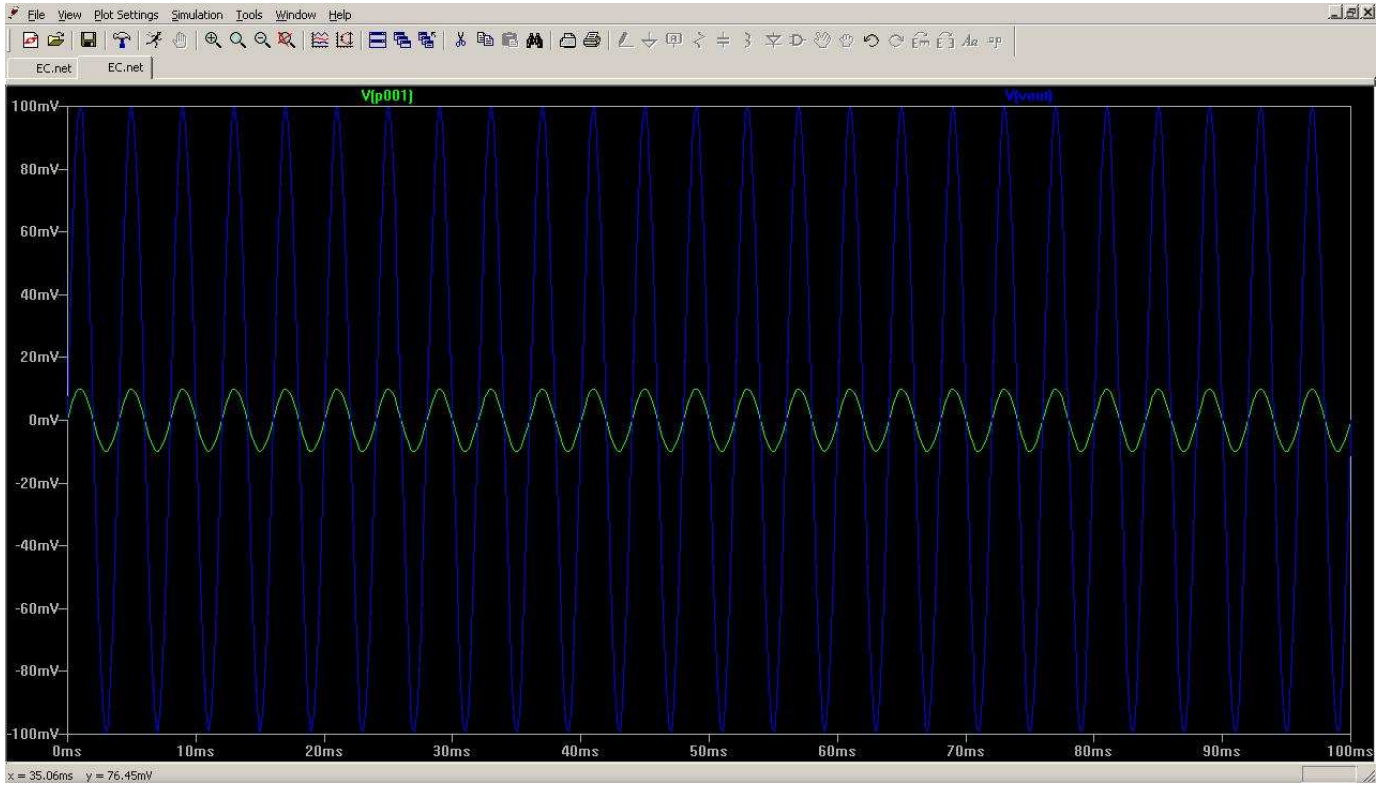


Fig. 5.  $V_{in}$  v/s  $V_{out}$  in Non-Inverting Op-amp

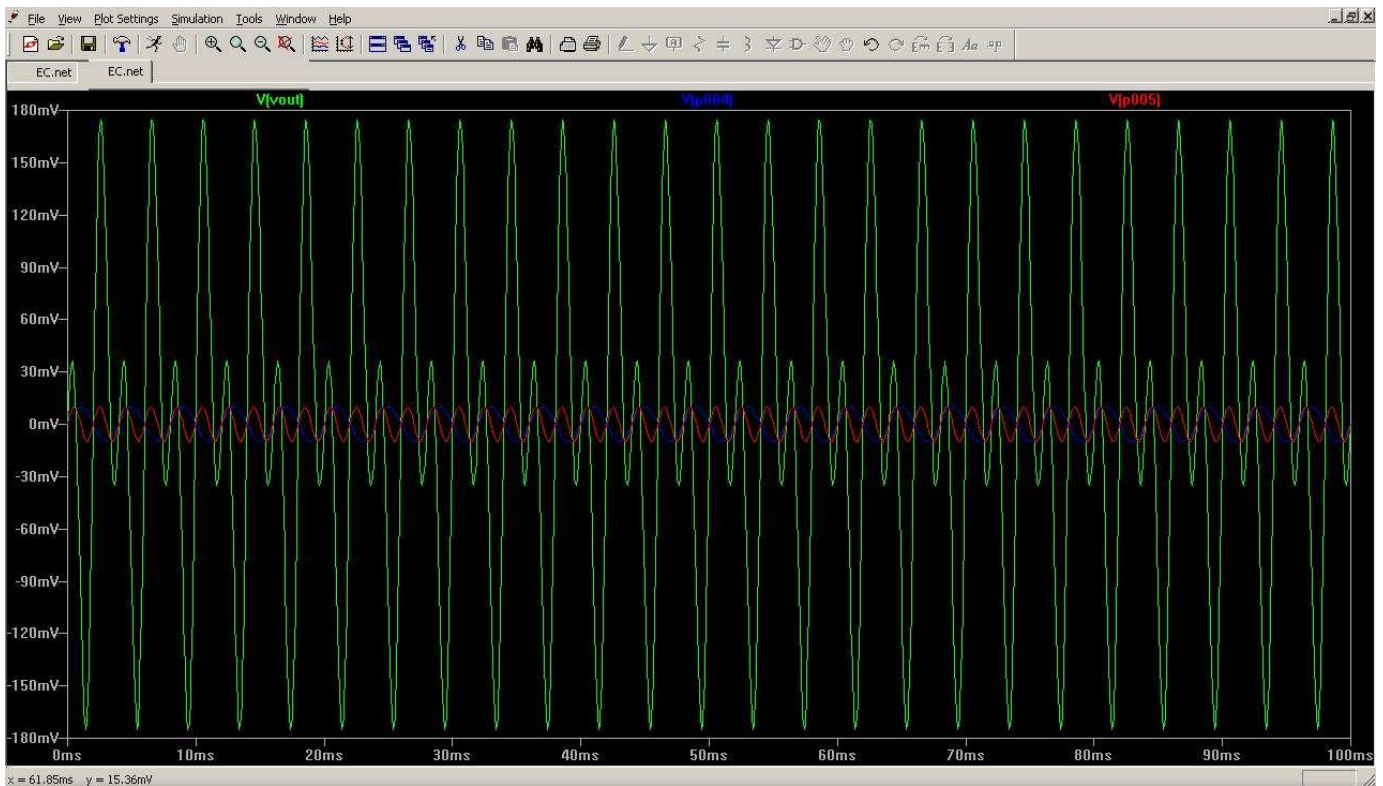


Fig. 6.  $V_{in}$  v/s  $V_{out}$  in Op-amp based Difference Amplifier

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## APPENDIX

### A. Design of single stage CE BJT Amplifier

We show the design of the common-emitter single stage BJT audio frequency amplifier.  $A_V$  and  $V_0$  is input by the user. We use voltage divider circuit as it provides Q point independent of temperature and beta. We use H-parameters of the CE BJT to analyse the circuit. The H parameters are  $h_{fe}$ ,  $h_{oe}$ ,  $h_{ie}$  and  $h_{re}$ , where  $h_{fe}$  is the current gain,  $h_{ie}$  is the input impedance and  $h_{oe}$  is the output admittance.

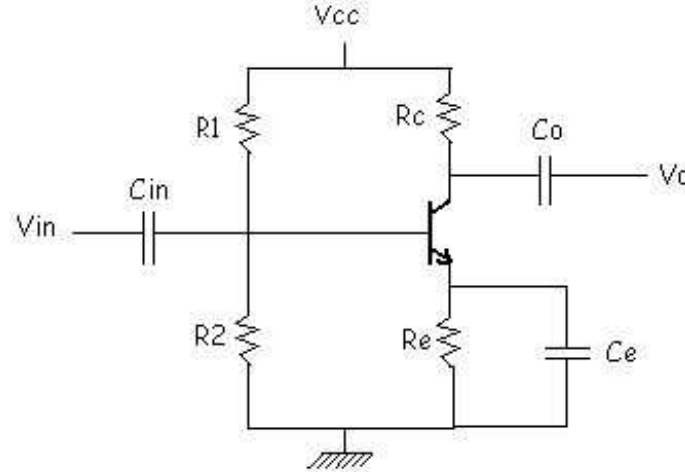


Fig. 7. Single stage BJT CE amplifier

#### Selection of $R_C$

$$R_{L'} = R_C \parallel R_L \quad (1)$$

If  $R_L$  not given,  $R_{L'} = R_C$

$R_L$  = load resistance connected between  $V_0$  and ground.

$$A_V = \frac{h_{fe} * R_{L'}}{h_{ie} + (h * R_C)} \quad (2)$$

Where

$$h = (h_{ie} * h_{oe}) - (h_{fe} * h_{re}) \quad (3)$$



We got  $h_{fe}$ ,  $h_{re}$ ,  $h_{ie}$ ,  $h_{oe}$  from data sheet [4].

$$h_{fe} = \beta, \quad h_{fe,max} = \beta_{max}, \quad h_{fe,min} = \beta_{min} \quad (4)$$

From the above equations we calculated  $R_{L'}$  and  $R_C$ . Select higher std value for  $R_C$  to increase voltage gain if min voltage gain is specified or nothing is specified. If max voltage gain is specified use lower std value. If some specific voltage gain is specified, use nearest std val.

*Selection of operating point ( $V_{CEQ}$ ,  $I_{CQ}$ )*

If  $V_{CC}$  is given,

$$V_{CEQ} = \frac{V_{CC}}{2} \quad (5)$$

If  $V_{CC}$  is not given,

$$V_{CEQ} = 1.5 * (V_{0,peak} + V_{CE,sat}) \quad (6)$$

Then,

$$I_{C,peak} = \frac{V_{0,peak}}{R_{L'}} \quad (7)$$

$$I_{CQ} = I_{C,peak} + I_{C,min} \quad (8)$$

Assume  $I_{C,min} = 0$  or  $0.005mA$

*Selection of  $R_e$*

If  $V_{CC}$  is not given, assume

$$V_{re} = 1$$

If  $V_{CC}$  is given,

$$V_{re} = 10\% \text{ of } V_{CC}$$

For either case,

$$R_e = \frac{V_{re}}{I_{CQ}} \quad (9)$$

Select lower std value of  $R_e$  so that voltage drop across  $R_e$  is less which increases the voltage swing of o/p.

*Selection of  $V_{CC}$*

If  $V_{CC}$  is not given,

$$V_{CC} = V_{CEQ} + I_{CQ} * (R_C + R_e) \quad (10)$$

Assume higher std val (typically 9,12,15,18).

*Selection of  $R_1$  and  $R_2$*

If stability factor is not given, assume  $s = 8$

$$s = \frac{1 + h_{fe,max}}{1 + \frac{h_{fe,max} * R_e}{R_b + R_e}} \quad (11)$$

$R_b$  is found and it is not standardized.

$$V_{r2} = V_{be} + V_{re} \quad V_{r1} = V_{CC} - V_{r2} \quad (12)$$

Assume  $V_{be} = 0.7 \text{ V}$  (for Si)

$$\frac{R_1}{R_2} = \frac{V_{r1}}{V_{r2}} \quad (13)$$



We get  $R_1$  in terms of  $R_2$ . Substitute in  $R_b$ .

$$R_b = R_1 \parallel R_2 = \frac{R_1 * R_2}{R_1 + R_2} \quad (14)$$

$R_2$  is found. Select lower standard value to make circuit independent of  $\beta$ . Substitute in (13) to find  $R_1$ . We should select higher standard value so that circuit draws minimum current from supply.

*Selection of coupling capacitors*

Select higher standard value for all capacitors.

*Selection of  $C_E$*

$$X_{CE} = \frac{R_e}{10} \quad (15)$$

$$C_E = \frac{1}{2 * \pi * f_L * X_{CE}} \quad (16)$$

where  $f_L$  = lower cutoff frequency. Assume  $f_L = 20$  Hz.

*Selection of  $C_B$*

If  $R_S$  (Source resistance) is not specified, assume  $R_S = 0$

$$X_{CB} = R_S + R_b \parallel h_{ie} \quad (17)$$

$$C_B = \frac{1}{2 * \pi * f_L * X_{CB}} \quad (18)$$

*Selection of  $C_C$*

$$R_b = R_1 \parallel R_2 \quad (19)$$

$$X_{CC} = R_C + R_L \quad (20)$$

If  $R_L$  (load resistance) is not specified, then we assume amplifier is connected to a similar next stage.

Hence,

$$R_L = R_b \parallel h_{ie} \quad (21)$$

$$C_C = \frac{1}{2 * \pi * f_L * X_{CC}} \quad (22)$$

### B. Design of two-stage BJT CE Amplifier

Value of  $A_V$  is input by the user.

Overall voltage gain,

$$A_V = A_{v1} * A_{v2} \quad (23)$$

$$\frac{A_{v1}}{A_{v2}} = \frac{R_{C1}}{R_{C2}} \quad (\text{Assumed})$$

$A_{v1}$  and  $A_{v2}$  can be found from the above equations.

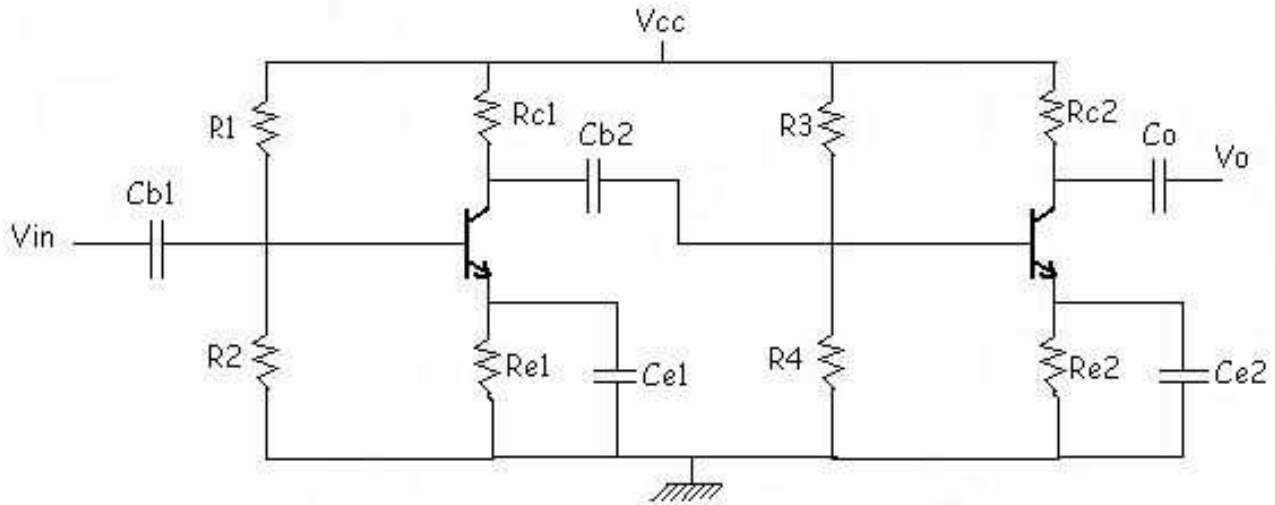


Fig. 8. Two-stage BJT CE amplifier

1) Part 1: Design of second stage: Calculation of  $R_L$ :

$$R_L = \frac{V_{0,peak}}{I_{0,peak}} \quad (24)$$

Not necessary if  $R_L$  is not given or  $V_{0,peak}$ ,  $I_{0,peak}$  is not given.

Selection of  $R_{C2}$ :

$$A_{v2} = \frac{h_{fe} * R_{L2'}}{h_{ie}} \quad (25)$$

$$R_{L'} = R_{C2} \parallel R_L \quad (26)$$

or, if  $R_L$  is not given, then,

$$R_{L'} = R_{C2} \quad (27)$$

Hence, we calculate  $R_L'$  and  $R_{C2}$

Selection of  $V_{CEQ}$ :

Case 1:  $V_{CC}$  is given

$$V_{CEQ,2} = 1.5 * (V_{0,peak} + V_{CE,saturation}) \quad (28)$$

If  $V_0$  is not given, then

$$V_{CEQ} = \frac{V_{CC}}{2} \quad (29)$$

$$V_{re2} = 10 \text{ to } 20 \% \text{ of } V_{CC} \quad (30)$$

$$V_{rc2} = V_{CC} - V_{CEQ,2} - V_{re2} \quad (31)$$

$$I_{CQ,2} = \frac{V_{rc2}}{R_{C2}} \quad (32)$$

$$R_{e2} = \frac{V_{re2}}{I_{CQ,2}} \quad (33)$$

Select lower standard value so that drop across  $R_e$  is less which increases gain of the output.

Case 2:  $V_{CC}$  is not given

$$V_{CEQ,2} = 1.5 * (V_{0,peak} + V_{CE,saturation}) \quad (34)$$

$$I_{C2,peak} = \frac{V_{0,peak}}{R_{L2}} \quad (35)$$

Assume  $V_{re2} = 2 \text{ V}$

$$V_{CC} = V_{CEQ} + I_{CQ} * (R_{C2} + R_{e2}) \quad (36)$$

Select higher std value.

Selection of  $R_3, R_4$

If stability factor is not given, assume  $s = 8$

$$s = \frac{h_{fe} + 1}{1 + \frac{h_{fe} * R_{e2}}{R_{b2} + R_{e2}}} \quad (37)$$

$R_b$  is found.

$$V_{r4} = V_{be} + V_{re} \quad (38)$$

$$V_{r3} = V_{CC} - V_{r2} \quad (39)$$

Assume  $V_{be} = 0.7\text{V}$  (for Si)

$$\frac{R_3}{R_4} = \frac{V_{r3}}{V_{r4}} \quad (40)$$

Get  $R_3$  in terms of  $R_4$  and substitute in  $R_{b2}$

$$R_{b2} = R_3 \parallel R_4 = \frac{R_3 * R_4}{R_3 + R_4} \quad (41)$$

Find  $R_4$ . Select lower standard value to make circuit independent of beta. Substitute in (40) to find  $R_3$ . Select higher standard value so that circuit draws minimum current from supply.

2) Part 2: Design of first stage:

$$A_{v1} = \frac{A_V}{A_{v2}} \quad (42)$$

Selection of  $R_{C1}$

$$A_{v1} = \frac{h_{fe} * R_{L1'}}{h_{ie}} \quad (43)$$

$$R_{L1'} = R_{C1} \parallel R_{b2} \parallel h_{ie} \quad (44)$$

$R_{L1'}$  and  $R_{C1}$  is calculated.

Let  $V_{CEQ,1} = V_{CEQ,2}$ ,  $V_{rc1} = V_{rc2}$ ,  $V_{re1} = V_{re2}$ ,  $I_{CQ,1} = \frac{V_{re1}}{R_{C1}}$  and  $R_{e1} = \frac{V_{re1}}{I_{CQ,1}}$

Selection of  $R_1, R_2$

$$s = \frac{1 + h_{fe,max}}{1 + \frac{h_{fe,max} * R_e}{R_b + R_e}} \quad (45)$$

$R_b$  is found.

$$V_{r2} = V_{be} + V_{re} \quad (46)$$

$$V_{r1} = V_{CC} - V_{r2} \quad (47)$$

Assume  $V_{be} = 0.7V$

$$\frac{R_1}{R_2} = \frac{V_{r1}}{V_{r2}} \quad (48)$$

We get  $R_1$  in terms of  $R_2$  and substitute in  $R_b$ .

$$R_b = R_1 \parallel R_2 = \frac{R_1 * R_2}{R_1 + R_2} \quad (49)$$

Find  $R_2$ . We select lower standard value to make circuit independent of  $\beta$ . Substitute in (48) to find  $R_1$ . Select higher standard value so that circuit draws minimum current from supply.

*Selection of coupling capacitors:* Select higher standard value for all capacitors.

*Selection of  $C_{E1}$ :*

$$X_{CE1} = \frac{R_{e1}}{10} \quad (50)$$

$$C_{E1} = \frac{1}{2 * \pi * f_L * X_{CE1}} \quad (51)$$

$f_L$  = lower cutoff frequency. We assume  $f_L = 20$  Hz.

*Selection of  $C_{E2}$ :*

$$X_{CE2} = \frac{R_{e2}}{10} \quad (52)$$

$$C_{E2} = \frac{1}{2 * \pi * f_L * X_{CE2}} \quad (53)$$

*Selection of  $C_{B1}$ :*

$$R_b = R_1 \parallel R_2 \quad (54)$$

If  $R_S$  (Source resistance) is not specified, assume  $R_S = 0$

$$X_{CB1} = R_b \parallel h_{ie} \quad (55)$$

$$C_{B1} = \frac{1}{2 * \pi * f_L * X_{CB}} \quad (56)$$

*Selection of  $C_{B2}$ :*

$$R_{b2} = R_3 \parallel R_4 \quad (57)$$

$$X_{CB2} = R_{C1} + R_b \parallel h_{ie} \quad (58)$$

$$C_{B2} = \frac{1}{2 * \pi * f_L * X_{CB}} \quad (59)$$

*Selection of  $C_0$ :*

$$R_{b2} = R_3 \parallel R_4 \quad (60)$$

$$X_{CC} = R_C + R_L \quad (61)$$

If  $R_L$  (load resistance) is not specified, then assume amplifier is connected to a similar next stage. Hence,

$$R_L = R_{b1} \parallel h_{ie} \quad (62)$$

$$C_C = \frac{1}{2 * \pi * f_L * X_{CC}} \quad (63)$$

### C. Design of Operational Amplifiers based Amplifiers

Depending upon whether the value of  $A_V$  input by the user is positive or negative, the circuit is interpreted to be of the configuration non-inverting or inverting, respectively.

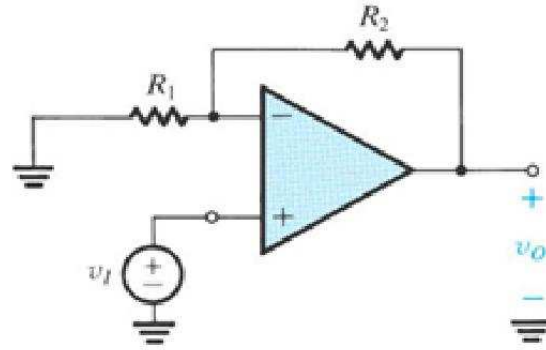


Fig. 9. Non-Inverting Operational Amplifier [7]

1) *Non-Inverting Amplifier*: The user inputs the gain  $A_V$  and the resistances  $R_1$  and  $R_2$  are found by the following formula :

$$A_V = 1 + \frac{R_2}{R_1} \quad (64)$$

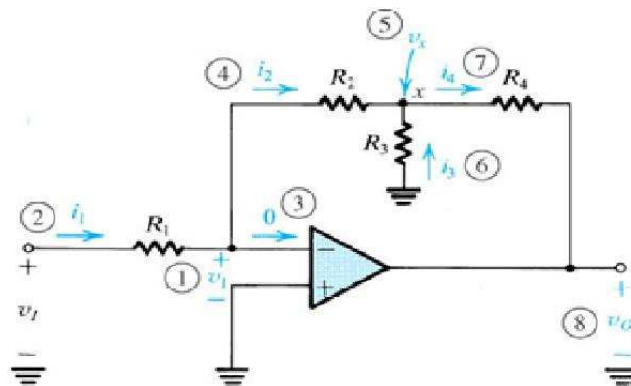


Fig. 10. Inverting Operational Amplifier [7]

2) *Inverting Amplifier*: At the inverting terminal of the op-amp, the voltage is

$$V_1 = -\frac{v_0}{A} = -\frac{v_0}{\infty} = 0 \quad (65)$$

Here we have assumed that the circuit is producing a finite output voltage  $v_0$ .

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1} \quad (66)$$

Since zero current flows into the inverting input terminal, all of  $i_1$  will flow through  $R_2$ , and thus :

$$i_2 = i_1 = \frac{v_{in}}{R_1} \quad (67)$$

Voltage at  $x$  :

$$V_x = v_1 - i_2 * R_2 = 0 - \frac{v_I}{R_1} * R_2 = -\frac{R_2}{R_1} * v_I \quad (68)$$

This in turn enables us to find  $i_3$  :

$$i_3 = \frac{0 - V_x}{R_3} = \frac{R_2}{R_1 * R_3} * v_I \quad (69)$$

Next, a node equation at  $x$  yields  $i_4$  :

$$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 * R_3} * v_I \quad (70)$$

Finally, we can determine  $v_0$  from

$$v_0 = V_x - i_4 * R_4 = \left(-\frac{R_2}{R_1}\right) * v_I - \left(\frac{v_I}{R_1} + \frac{R_2}{R_1 * R_3} * v_I\right) * R_4 \quad (71)$$

Thus, the voltage gain is given by :

$$\frac{v_0}{v_I} = \frac{R_2}{R_1} + \frac{R_4}{R_1} * \left(1 + \frac{R_2}{R_3}\right) \quad (72)$$

which can be written in the form

$$\frac{v_0}{v_I} = -\frac{R_2}{R_1} * \left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right) \quad (73)$$

#### D. Design of Op-Amp based Difference Amplifier

User inputs  $A_d$ .

In ideal case,

$$A_{CM} = 0 \quad \text{and} \quad A_d = \frac{R_2}{R_1} \quad (74)$$

#### E. Design of Power Amplifier Class A

Selection of operating point :

$$V_{re} = \frac{V_{CC}}{10} \quad (75)$$

$$V_{CEQ} = V_{CC} - V_{re} \quad (76)$$

$$V_{CE,peak} = V_{CEQ} - V_{CE,sat} \quad (77)$$

$$I_{C,peak} = \frac{2 * P_{L'}}{V_{CE,peak}} \quad (78)$$

$$I_{CQ} = I_{C,peak} + I_{C,min} \quad (79)$$

Assume  $I_{C,min} = 0$ .

Hence, we calculate  $I_{CQ}$

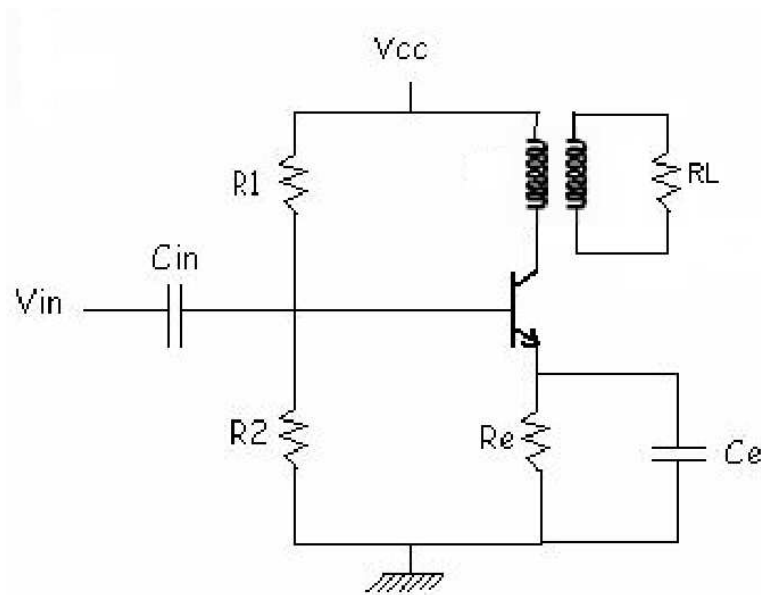


Fig. 11. Power Amplifier Class A

*Selection of  $R_e$  and  $C_e$  :*

$$R_e = \frac{V_{re}}{I_{CQ}} \quad (80)$$

$$P_{re} = \frac{V_{re}^2}{R_e} \quad (81)$$

$$C_e = \frac{1}{2 * \pi * f_L * R_L} \quad (82)$$

We assume  $f_L = 50$  Hz. Since  $C_e$  is very high, we leave  $R_e$  unbypassed.

*Selection of  $R_1$  and  $R_2$  :*

Assume  $s = 10$

$$s = \frac{1 + h_{fe,max}}{1 + \frac{h_{fe,max} * R_e}{R_b + R_e}} \quad (83)$$

$R_b$  is found.

$$V_{r2} = V_{be} + I_{CQ} * R_e \quad (84)$$

$$V_{r1} = V_{CC} - V_{r2} \quad (85)$$

Assume  $V_{be} = 0.7V$

$$\frac{R_1}{R_2} = \frac{V_{r1}}{V_{r2}} \quad (86)$$

We get  $R_1$  in terms of  $R_2$  and then substitute in  $R_b$

$$R_b = R_1 \parallel R_2 = \frac{R_1 * R_2}{R_1 + R_2} \quad (87)$$

$R_2$  is found. Select lower standard value to make circuit independent of  $\beta$ . Then it is substituted in (86) to find  $R_1$ . Select higher standard value so that circuit draws minimum current from supply.



*Selection of output transformer :*

$$R_{L'} = \frac{V_{CE,peak}}{I_{C,peak}} \quad (88)$$

$R_{L'}$  is calculated.

$$R_{L'} = \frac{N_1^2}{N_2^2} * R_L \quad (89)$$

$\frac{N_1}{N_2}$  is calculated.